

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

Harlan T. Beverly et al.

Serial No.:

10/081,748

Filed:

February 22, 2002

For:

Synchronizing and Converting
the Size of Data Frames

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Art Unit:

2662

Examiner:

Habte Mered

Docket:

ITL 0703US
P13939

Assignee:

Intel Corporation

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF PERCY WONG

Sir:

I, Percy Wong, do declare as follows:

1. I am an inventor of U.S. patent application 10/081,748, filed February 22, 2002 for Synchronizing and Converting the Size of Data Frames.
2. I am employed by Intel Corporation, the Assignee of the application.
3. A true and correct copy of an invention disclosure related to the above application is attached as Exhibit A. Exhibit A was prepared before October 12, 2001. The dates on the document are redacted.
4. Exhibit A shows all of the elements of claim 1, including receiving a data frame of a first size, such as 64 bits, de-multiplexing the data frame, writing blocks of the de-multiplexed data frame at the first size into a register, reading blocks of a second data size, different from the

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first data size from the register multiplexing said blocks to form an output data frame of a second size. This is shown in Figure 1 of the disclosure where the input data size is 64 bits, the output data size is 64 bits, a 1:33 de-mux is for de-multiplexing the data frame, a register 2112 is the register that the blocks are written into after de-multiplexing at the first size and the multiplexer is the 32:1 multiplexer also shown in Figure 1. The elements of claim 11 are also shown. The subject matter of claims 1-22 was invented prior to October 12, 2001.

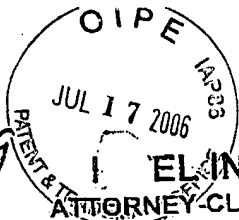
5. The invention disclosure to obtain patent protection was submitted before October 12, 2001. I never intended to abandon, suppress, or conceal my invention.

6. I declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date:

6-28-06


Percy Wong



INVENTION DISCLOSURE

 ATTORNEY-CLIENT PRIVILEGED COMMUNICATION
 located at <http://legal.intel.com>

DATE:

PATENT DATABASE GROUP

INTEL LEGAL TEAM

It is important to provide accurate and detailed information on this form. The information you provide on this form will be used by the Legal Department to determine if your invention is eligible for patent protection. When completed and signed, please return this form to the Legal Department at JF3-147. You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval. If you have any questions, please call 264-0444.

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*If you are unsure of this information, please discuss with your manager.

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Method of converting a 64-bit frame into a 66-bit frame
3. What technology/product/process (code name) does it relate to (be specific if you can):
Ethernet, Networking
4. Include several key words to describe the technology area of the invention in addition to # 3 above: 10Gigabit, IEEE802.3ae, 10GBASE-R, 64B/66B code, Physical Coding Sublayer (PCS)
5. Stage of development (i.e. % complete, simulations done, test chips if any, etc.): 100% complete, simulations done. Tapeout is December 2001
6. (a) Has a description of your invention been, or will it shortly be, published outside Intel:
 NO: ☒ YES: ☐ IF YES, was the manuscript submitted for pre-publication approval? ☐
 IDENTIFY THE PUBLICATION AND THE DATE PUBLISHED: _____
- (b) Has your invention been used/sold or planned to be used/sold by Intel or others?
 NO: ☐ YES: ☒ DATE WAS OR WILL BE SOLD: December 2001 Engineering Samples

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(c) Does this invention relate to technology that is or will be covered by a SIG (special interest group), standard, or specification?

NO: _____ YES: X Name of SIG/Standard/Specification: IEEE802.3ae

(d) If the invention is embodied in a semiconductor device, actual or anticipated date of tapeout? December 2001

(e) If the invention is software, actual or anticipated date of any beta tests outside Intel N/A

7. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia? NO: X YES: _____ Name of individual or entity: _____

8. Is this invention related to any other invention disclosure that you have recently submitted? If so, please give the title and inventors: N/A

**PLEASE READ AND FOLLOW THE DIRECTIONS ON
HOW TO WRITE A DESCRIPTION OF YOUR INVENTION**

Please attach a description of the invention to this form and include the following information:

1. Describe in detail what the components of the invention are and how the invention works.
2. Describe advantage(s) of your invention over what is done now.
3. YOU MUST include at least one figure illustrating the invention.
If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.
4. Value of your invention to Intel (how will it be used?).
5. Explain how your invention is novel. If the technology itself is not new, explain what makes it different.
6. Identify the closest or most pertinent prior art that you are aware of.
7. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

**HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM
OR FORWARD IT ELECTRONICALLY VIA E-MAIL TO "INVENTION DISCLOSURE SUBMISSION"**

DATE: _____ SUPERVISOR: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

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3. Figures or Flowcharts

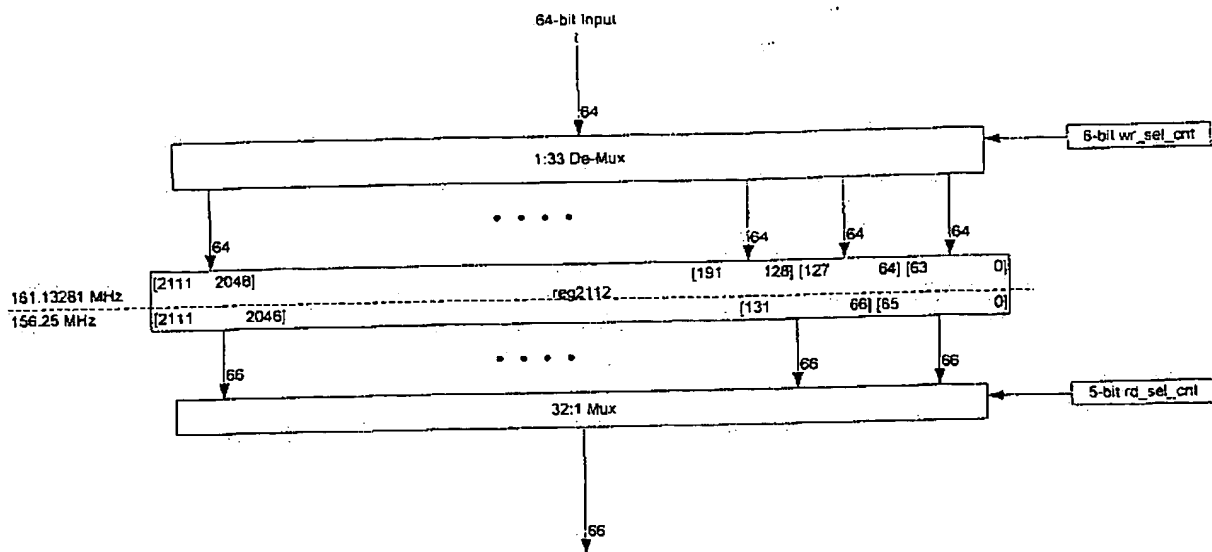


Figure 1: The 64-bit to 66-bit Converter

4. Value to Intel

This design is critical to all 10Gig products that conform to the IEEE802.3ae standard that supports 10GBASE-R. It is being used by the Calypso project.

5. Novelty

It is novel in the sense that its purpose was really never needed before until the IEEE802.3ae standard started working out solutions for 10Gigabit Ethernet. The standard basically requires that a solution be able to convert a 16-bit data frame into a 66-bit data frame. In this design, the 16-bit data is clocked at ~644 MHz and is converted to 64-bit data frames. This high-speed bus converter is handled by custom IP logic. The 64-bit data frame is then required to be converted to a 66-bit data frame. It is here that this solution becomes novel in being able to solve this conversion.

6. Prior Art

None.

7. Who use/ Detection

It would be difficult to detect use of this implementation in hardware or software without some form of silicon reverse engineering.

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Method of Converting A 64-bit Frame Into A 66-bit Frame

By: Harlan T. Beverly & Percy Wong

1. Description

This invention is part of the IEEE802.3ae Physical Coding Sub-layer (PCS) implementation. It is a solution to the 64B/66B coding scheme. The purpose of the 64B/66B encoding/decoding scheme is to preserve the integrity of the information and allow for later synchronization. The basic function of this invention is to reliably convert streaming 64-bit frames of data into 66-bit frames of data without losing bits or causing any stalls. The invention uses a 2112-bit register. The conversion occurs by having 64-bit writes to the 2112-bit register occur at a clock frequency of 161.13281 MHz. This same register is simultaneously read at 66-bit blocks at a clock frequency of 156.25 MHz. This calculated data width and frequency allows for a seamless conversion. A write pointer clocked at 161.13281 MHz controls where within the 2112-bit register the next 64-bit block is written. Likewise, a read pointer clocked at 156.25 MHz controls where the next 66-bit read is to occur. There are specific 64 bit lanes on the write side and specific 66 bit lanes on the read side. The 2112-bit register is chosen because it allows for an exact multiple of both 64 and 66, or 33 64bit locations which is equivalent to 32 66bit locations. This allows for lanes to directly map to 64 bits on the "write" side and 66 bits on the "read" side. Muxes are used to direct where the write and read is to occur.

2. Advantages

The advantages of this method are its simplicity and reliability. Its components consist of a large register, multiplexers, and two counters. It also provides a solution necessitated by the IEEE802.3ae standard for 10GBASE-R.

Another advantage is that it relaxes timing requirements of each mux because there is a register between the two muxes, effectively halving the timing requirements of each mux.

The final advantage of this method is that by keeping the read and write pointers separated (creating a buffer), this method allows for any minor clock skews which may occur in the system.

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